



AM-ASB TLA Logic Analyzer Instruction Manual

Support for
ARM Microprocessors
with an AMBA-ASB Bus

Software Version 1.0

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About This Manual

This manual describes the features of the AM-ASB TLA Logic Analyzer Support Package including:

- Features of the support package
- Package installation
- Configuration
- Guidelines for connecting to the system under test

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Support Description

The AM-ASB Support Package provides timing analysis, state analysis and both ARM and Thumb disassembly support for ARM microprocessor cores. This package is designed to capture and analyze the AMBA-ASB bus activity of an ARM processor.

Since the ARM is a microprocessor core, it is not possible to provide a support package that will work correctly with all possible ARM configurations, due to specific ASIC implementation differences which might arise. However, this support is compatible with the AMBA-ASB specification, and is designed to operate directly on the ARM Integrator development boards, as well as other boards that provide access to the required address, data and bus control signals.

The AM-ASB Support Package runs on mainframes equipped with logic analyzer modules that are 102 channels or wider. At the time this manual was printed, the supported logic analysis modules include the TLA7L3, TLA7M3, and TLA7N3 102 channel modules, and the TLA7L4, TLA7M4, TLA7N4 and TLA7P4 136 channel modules.

Support Features

This package is designed to operate on the AMBA-ASB bus. In addition to the timing and state analysis support, this package provides disassembly support for both ARM and Thumb instructions, in both little and big endian modes. ARM/Thumb detection is automatic.

Support-required Signals

The following signals should be provided to the logic analyzer module in order to support the ARM on AMBA-ASB bus:

SIGNAL	REQUIRED?	EFFECT IF SIGNAL NOT AVAILABLE
BCLK	Strongly Recommended	Internal or External clocking must be used to acquire bus cycles.
BWAIT	Strongly Recommended	Bus wait state cycles will be acquired and disassembled, even though the bus cycle is not appropriate for disassembly.
BTRAN[1]	Recommended	Address-only bus cycles will be acquired and disassembled, even though the bus cycle is not appropriate for disassembly.
BD[31-0]	Yes	No disassembly.
BA[31-2]	Optional	Disassembled address values will be incorrect.
BA[1]	Strongly Recommended	Disassembly of Thumb instructions and display of 16-bit data transfers will be inaccurate.
BA[0]	Recommended	Display of 8-bit data transfers will be inaccurate.
BFSIZE[1:0]	Strongly Recommended	ARM/Thumb disassembly support is degraded, as is identification of data transfer sizes.
BWRITE	Recommended	Data transfer direction will be misidentified.
BPROT[1]	Optional	No impact on disassembly.
BPROT[0]	Strongly Recommended	No automatic detection of instruction fetch bus cycles.

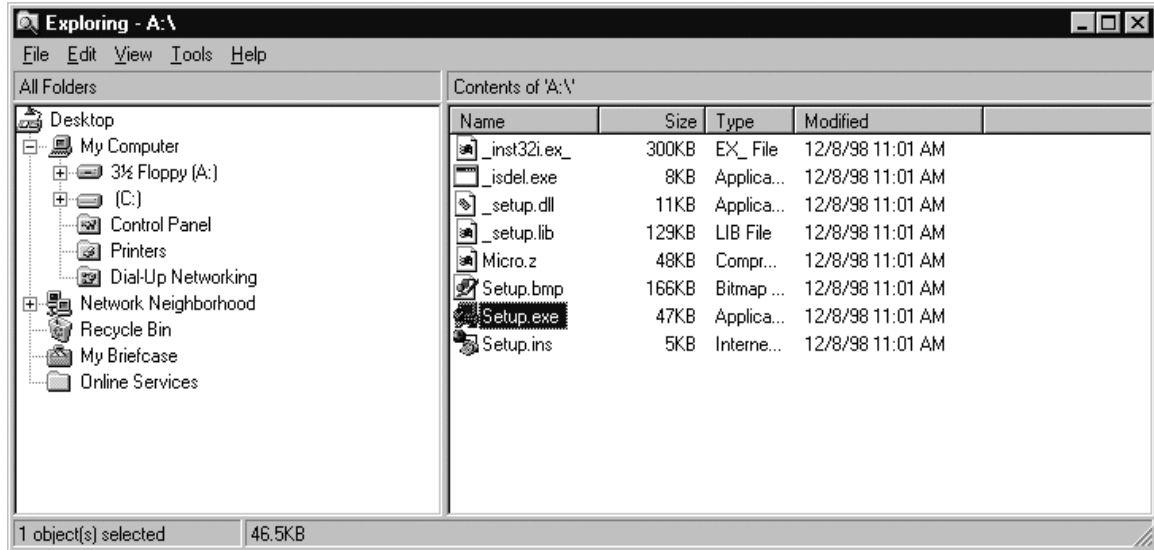
*Configuring the AM-ASB Support
Package*

Installing the AM-ASB TLA Support Package

Place the AM-ASB installation disk in the mainframe floppy disk drive. Click on the Windows 95/98 Start icon and select the Windows Explorer program. Click on the 3 ½” Floppy icon to see the contents of the application software installation disk, and then double-click on the Setup.exe file to start the installation process.

The installation program will automatically install the package software into the appropriate folders in the file system. For the AM-ASB package, the support files will be installed into the “C:/Program Files/TLA700/Supports/AM-ASB” folder.

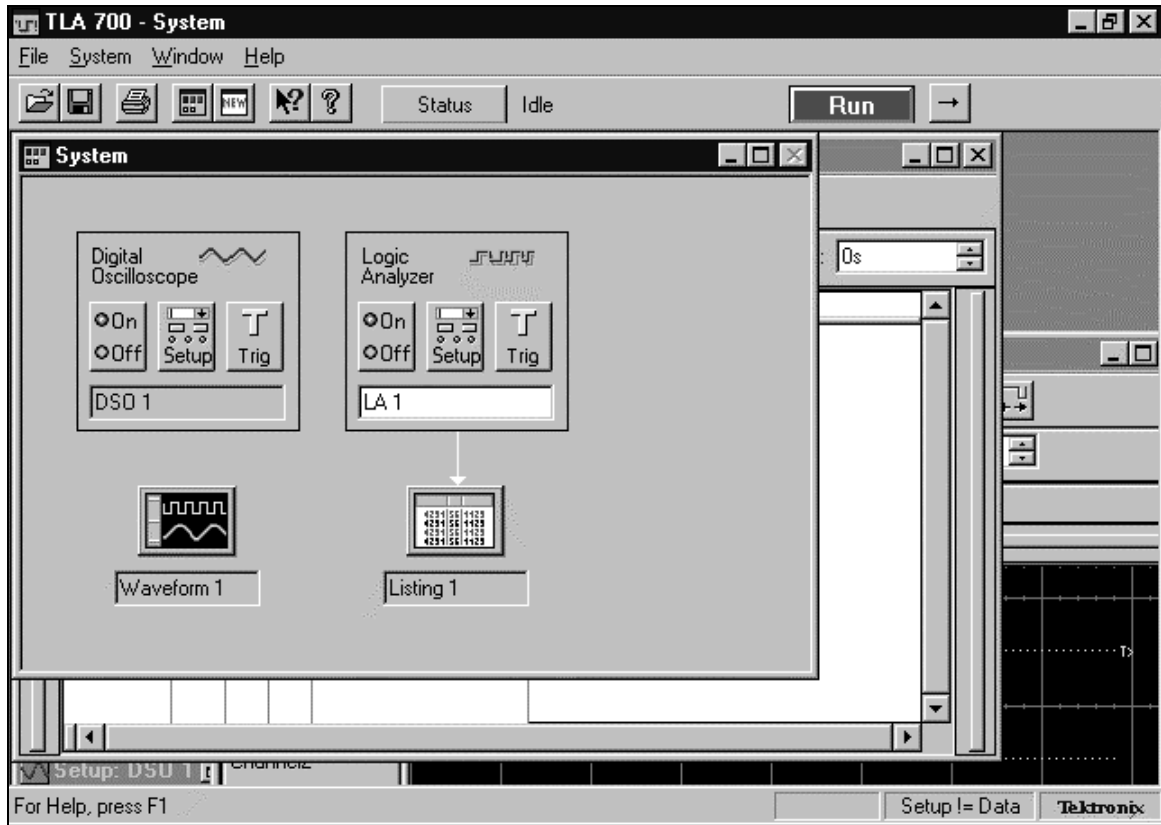
FIGURE 1. Double-click on the Setup.exe icon to install the software



Loading the AM-ASB Support Package

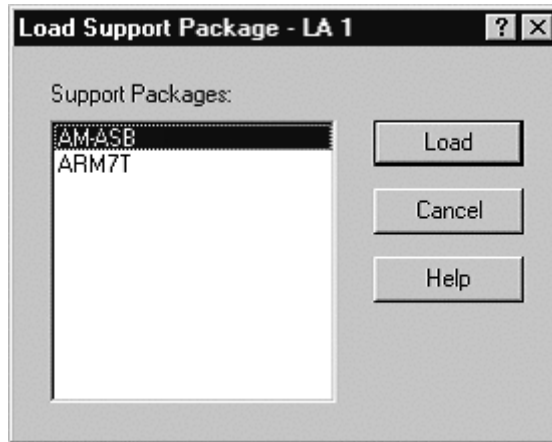
To Load the AM-ASB support package you must first select the logic analysis module that will be connected to the bus under test. In the System menu, select the logic analysis module by clicking on the title bar (labeled LA 1 below). This field will be renamed to the name of the supported microprocessor, in this case AM-ASB, after successfully loading the support software.

FIGURE 2. Selecting the logic analysis module for loading AM-ASB support software.



Now click File in the toolbar and select the Load Support Package option. The menu shown in Figure 3 will pop up on screen, allowing you to pick the support package you wish to load into the logic analysis module. Note that the list of support packages shown will depend on which microprocessor support applications you have previously loaded into the TLA

FIGURE 3. Load Support Package Dialog Box



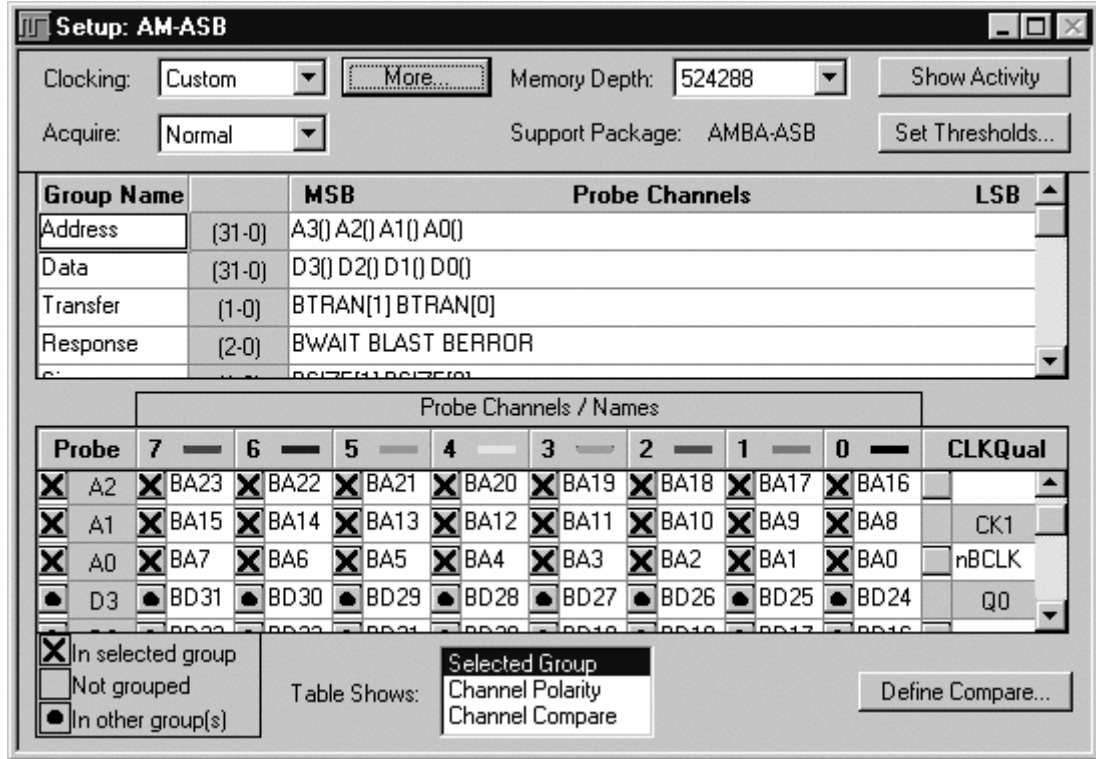
Select AM-ASB from the list of available support packages, and then click on the Load button. A dialog box with the following text will appear on screen:

Loading a support package invalidates a module's acquired data. Do you wish to save the current module's settings and data before loading the support package?

If you choose Yes, a "Save As..." file dialog box will appear, allowing you to save your current module setup or setup and data. Selecting No will cause the TLA to overwrite your current setup and data with the support package setup.

Clicking on the Setup button for the logic analysis module will take you to the Setup menu shown in Figure 4. Note that all of the input channels to be connected to the microprocessor bus have already been grouped and named.

FIGURE 4. Logic analysis module setup after support has been loaded



Connecting to the AMBA-ASB Bus

The table below shows how to connect the logic analyzer cables on the Integrator/AM Module.

Cable	Integrator/AM Module
Address	ADDR (POD2)
Data	DATA (POD4)
Control	CONTROL1 (POD6)

If Your Module is Not One of the Officially Supported Boards

This logic analyzer is designed for use with P6434 Mictor connectors adhering to the Mictor pinout specification published by ARM Ltd. If your ARM board uses the same pinout specification, the AM-ASB Support Package will function correctly.

If you are building a new board and want to use the AM-ASB Support Package, design the pinouts according to the Mictor pinout specification. For details of the specification, see the *ARM Integrator/AM User Guide*, available at www.arm.com.

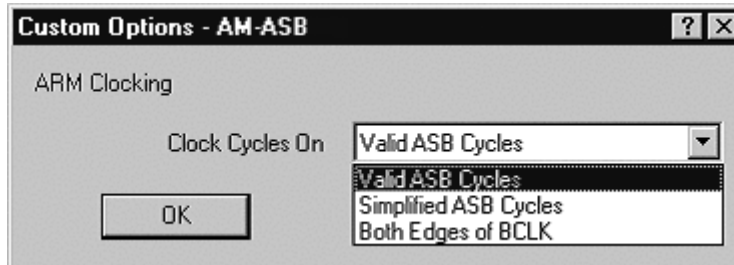
If your module does not adhere to the Mictor pinout specification NEX-HDSWIZ adapters are available from New Wave PDG. See www.busboards.com for adaptor specifications and ordering information.

The Mictor connector is described in Tektronix document 070-9793-02, available from Tektronix, at <http://www.tek.com>.

Clocking Options for the AM-ASB Support Package

The AM-ASB Support Package provides several customized clocking options that are tailored to the characteristics of the AMBA-ASB bus. Clicking on the More... button shown in the Setup menu in Figure 4 will take you to the Custom Clocking Options dialog box, shown below in Figure 5.

FIGURE 5. Custom Clock Options dialog box.



The following clocking options are available:

- Valid ASB Cycles** This is the most commonly used of the clocking options, and is recommended for conforming AMBA-ASB bus implementations. With this clocking option, BWAIT is utilized to suppress bus wait state cycles, and BTRAN[1] is utilized to suppress address-only bus cycles.
- Simplified ASB Cycles** This clocking option is identical to “Valid ASB cycles”, except that BTRAN[1] is not utilized to suppress address-only bus cycles.
- Both Edges of BCLK** This clocking option samples the address, control, and data groups on both the rising and falling edges of BCLK. This clocking option is useful for debugging purposes, and can be used along with the Waveform displays of the TLA to study low-level AMBA-ASB bus activity.

The following signals are required for each clocking option:

Custom Clocking Option	BCLK	BWAIT	BTRAN[1]
Both Edges of BCLK	•		
Simplified ASB Cycles	•	•	
Valid ASB Cycles	•	•	•

These clocking options should allow the support package to acquire relevant AMBA-ASB bus activity in the majority of cases, but will not necessarily be appropriate for all implementations, due to implementation-specific differences in bus architecture, signal timing, etc. If a customized clocking method is required for a specific implementation, contact Dragonfly Software Development for information about adding additional support to the package. See “If You Need Assistance” for more information.

*Channel Groups and
Assignments*

Address Group

Group (Radix)	Group Bit Position, Section: Channel, & Channel Name			Voltage, Polarity	Mictor Conn./ Pin (Tek #)
Address (Hex)	31	A3:7	BA31	TTL,+	A4
	30	A3:6	BA30	TTL,+	A5
	29	A3:5	BA29	TTL,+	A6
	28	A3:4	BA28	TTL,+	A7
	27	A3:3	BA27	TTL,+	A8
	26	A3:2	BA26	TTL,+	A9
	25	A3:1	BA25	TTL,+	A10
	24	A3:0	BA24	TTL,+	A11
	23	A2:7	BA23	TTL,+	A12
	22	A2:6	BA22	TTL,+	A13
	21	A2:5	BA21	TTL,+	A14
	20	A2:4	BA20	TTL,+	A15
	19	A2:3	BA19	TTL,+	A16
	18	A2:2	BA18	TTL,+	A17
	17	A2:1	BA17	TTL,+	A18
	16	A2:0	BA16	TTL,+	A19
	15	A1:7	BA15	TTL,+	A35
	14	A1:6	BA14	TTL,+	A34
	13	A1:5	BA13	TTL,+	A33
	12	A1:4	BA12	TTL,+	A32
	11	A1:3	BA11	TTL,+	A31
	10	A1:2	BA10	TTL,+	A30
	9	A1:1	BA9	TTL,+	A29
	8	A1:0	BA8	TTL,+	A28
	7	A0:7	BA7	TTL,+	A27
	6	A0:6	BA6	TTL,+	A26
	5	A0:5	BA5	TTL,+	A25
	4	A0:4	BA4	TTL,+	A24
	3	A0:3	BA3	TTL,+	A23
	2	A0:2	BA2	TTL,+	A22
	1	A0:1	BA1	TTL,+	A21
	0	A0:0	BA0	TTL,+	A20

Data Group

Group (Radix)	Group Bit Position, Section: Channel, & Channel Name			Voltage, Polarity	Mictor Conn./ Pin (Tek #)
Data (Hex)	31	D3:7	BD31	TTL,+	D4
	30	D3:6	BD30	TTL,+	D5
	29	D3:5	BD29	TTL,+	D6
	28	D3:4	BD28	TTL,+	D7
	27	D3:3	BD27	TTL,+	D8
	26	D3:2	BD26	TTL,+	D9
	25	D3:1	BD25	TTL,+	D10
	24	D3:0	BD24	TTL,+	D11
	23	D2:7	BD23	TTL,+	D12
	22	D2:6	BD22	TTL,+	D13
	21	D2:5	BD21	TTL,+	D14
	20	D2:4	BD20	TTL,+	D15
	19	D2:3	BD19	TTL,+	D16
	18	D2:2	BD18	TTL,+	D17
	17	D2:1	BD17	TTL,+	D18
	16	D2:0	BD16	TTL,+	D19
	15	D1:7	BD15	TTL,+	D35
	14	D1:6	BD14	TTL,+	D34
	13	D1:5	BD13	TTL,+	D33
	12	D1:4	BD12	TTL,+	D32
	11	D1:3	BD11	TTL,+	D31
	10	D1:2	BD10	TTL,+	D30
	9	D1:1	BD9	TTL,+	D29
	8	D1:0	BD8	TTL,+	D28
	7	D0:7	BD7	TTL,+	D27
	6	D0:6	BD6	TTL,+	D26
	5	D0:5	BD5	TTL,+	D25
	4	D0:4	BD4	TTL,+	D24
	3	D0:3	BD3	TTL,+	D23
	2	D0:2	BD2	TTL,+	D22
	1	D0:1	BD1	TTL,+	D21
	0	D0:0	BD0	TTL,+	D20

Control Group

Group (Radix)	Group Bit Position, Section: Channel, & Channel Name			Voltage, Polarity	Mictor Conn./Pin (Tek#)
Control (SYM)	4	C2:0	BWRITE	TTL,+	C19
	3	C2:4	BSIZE[1]	TTL,+	C15
	2	C2:3	BSIZE[0]	TTL,+	C16
	1	C2:2	BPROT[1]	TTL,+	C17
	0	C2:1	BPROT[0]	TTL,+	C18
Transfer	1	Clock_0	BTRAN[1]	TTL,+	A3
	0	C0:0	BTRAN[0]	TTL,+	C20
Port	1	C2:2	BPROT[1]	TTL,+	C17
	0	C2:1	BPROT[0]	TTL,+	C18
Response	2	Qual_0	BWAIT	TTL,+	D3
	1	C3:0	BLAST	TTL,+	C11
	0	C2:7	BERROR	TTL,+	C12
Size	1	C2:4	BSIZE [1]	TTL,+	C15
	0	C2:3	BSIZE [0]	TTL,+	C16
(Not in group)		Clock_2	BCLK	TTL,+	D36

Overview of the Symbol Tables

Five symbol files are provided in this support package. Only one is displayed by default and is related to the Control group. The Control symbol table contains patterns that identify the type of valid bus transaction cycles for the symbolic disassembly. This symbol table is automatically selected for use in defining Control group patterns in the logic analyzer module's trigger menu as shown.

Symbol Table for the Control Group

Symbol name	Signals					Description
	BWRITE	BSIZE[1]	BSIZE[0]	BPROT[1]	BPROT[0]	
FETCH_U_B	0	0	0	0	0	byte fetch in User Access (unused)
READ_U_B	0	0	0	0	1	byte read in User Access
FETCH_S_B	0	0	0	1	0	byte fetch in Supervisor Access (unused)
READ_S_B	0	0	0	1	1	byte read in Supervisor Access
FETCH_U_H	0	0	1	0	0	halfword fetch in User Access (Thumb code)
READ_U_H	0	0	1	0	1	halfword read in User Access
FETCH_S_H	0	0	1	1	0	halfword fetch in Supervisor Access (Thumb code)
READ_S_H	0	0	1	1	1	halfword read in Supervisor Access
FETCH_U_W	0	1	0	0	0	word fetch in User Access (ARM code)
READ_U_W	0	1	0	0	1	word read in User Access
FETCH_S_W	0	1	0	1	0	word fetch in Supervisor Access (ARM code)
READ_S_W	0	1	0	1	1	word read in Supervisor Access
WRITE_U_B	1	0	0	0	1	byte write in User Access
WRITE_S_B	1	0	0	1	1	byte write in Supervisor Access
WRITE_U_H	1	0	1	0	1	halfword write in User Access
WRITE_S_H	1	0	1	1	1	halfword write in Supervisor Access
WRITE_U_W	1	1	0	0	1	word write in User Access
WRITE_U_W	1	1	0	1	1	word write in Supervisor Access
Undefined	X	X	X	X	X	undefined

Other symbol tables are available for the groups that are defined:

- The **Am-ASB_Tran.tsf** symbol file is used by the **Transfer group**.
- The **Am-ASB_Size.tsf** symbol file is used by the **Size group**.
- The **Am-ASB_Resp.tsf** symbol file is used by the **Resp group**.
- The **Am-ASB_Prot.tsf** symbol file is used by the **Prot group**.

To add a new group to a Listing window:

1. Select the Listing window that you want to modify, then click Edit,
2. Select “Add Column...” to bring up a list of the available groups.
3. Select the group that you wish to add to the Listing window, then click Add.

Symbol Table for the Transfer Group

Symbol name	Signals		Description
	BTRAN[1]	BTRAN[0]	
ADDRESS	0	0	Address cycle
RESERVED	0	1	Reserved
NONSEQ	1	0	Non-sequential cycle
SEQ	1	1	Sequential cycle

Symbol Table for the Size Group

Symbol name	Signals		Description
	BSIZE[1]	BSIZE[0]	
BYTE	0	0	8-bit access
HALF	0	1	16-bit access
WORD	1	0	32-bit access
RESERVED	1	1	Reserved

Symbol Table for the Resp Group

Symbol name	Signals			Description
	BWAIT	BLAST	BERROR	
DONE	0	0	0	Complete transfer successful
ERROR	0	0	1	Complete transfer error
LAST	0	1	0	Complete cannot continue with Burst
RETRACT	0	1	1	Complete bus retract
WAIT	1	0	0	Incomplete Insert Wait Cycle
resrvd	1	0	1	Reserved
resrvd	1	1	0	Reserved
RETNEXT	1	1	1	Bus retract next cycle

Symbol Table for the Prot Group

Symbol name	Signals		Description
	BPROT[1]	BPROT[0]	
U_OPCODE	0	0	Opcode Fetch - User Access
S_OPCODE	1	0	Opcode Fetch- Supervisor Access
U_DATA	0	1	Data Access
S_DATA	1	1	Data Access

Displaying Disassembled Data

Once the AM-ASB support package has been loaded, the Listing display for the logic analysis module will automatically display disassembled data. Figure 6 shows an example of disassembled data for an ARM microprocessor on AMBA-ASB:

FIGURE 6. Disassembled data display on the AMBA-ASB bus

Sample	AM-ASB Address	AM-ASB Data	AM-ASB Mnemonics	AM-ASB Control	Transfer
32	0007EDDC	00000000	(32bit DATA READ)	READ_S_W	SEQ
33	0007EDE0	000700E6	(32bit DATA READ)	READ_S_W	SEQ
34	0007EDE4	00000000	(32bit DATA READ)	READ_S_W	SEQ
35	0007EDE8	00000000	(32bit DATA READ)	READ_S_W	SEQ
36	0007EDEC	01007CD4	(32bit DATA READ)	READ_S_W	ADDRESS
37	01000398	01007CD4	(32bit DATA READ)	READ_S_W	SEQ
38	01000398	13511F00	CMPNE R1,#0x00	FETCH_S_W	SEQ
39	0100039C	028D0400	ADDEQ RO,SP,#0x00000000	FETCH_S_W	SEQ
40	010003A0	18B00200	LDMNEFD SP!,[R9]	FETCH_S_W	SEQ
41	010003A4	116901F0	STRNESH RO,[R9,#-0x10]!	FETCH_S_W	SEQ
42	010003A8	E3102000	TST RO,#0x00	FETCH_S_W	NONSEQ
43	0007EDF0	00000000	(32bit DATA READ)	READ_S_W	ADDRESS
44	010003AC	00000000	(32bit DATA READ)	READ_S_W	SEQ
45	010003AC	0A000400	BEQ 0100E3B4	FETCH_S_W	SEQ
46	010003B0	E3C02000	(FLUSH)	FETCH_S_W	SEQ
47	010003B4	E12900F0	(FLUSH)	FETCH_S_W	NONSEQ
48	010003C4	E2001F10	AND R1,RO,#0x40	FETCH_S_W	SEQ
49	010003C8	E3511000	CMP R1,#0x00	FETCH_S_W	SEQ
50	010003CC	0A000400	BEQ 0100E3D4	FETCH_S_W	SEQ
51	010003D0	E3511F00	CMP R1,#0x00	FETCH_S_W	SEQ
52	010003D4	0A000200	BEQ 0100DB0C	FETCH_S_W	SEQ
53	010003D8	E16900F0	STRSH RO,[R9]	FETCH_S_W	SEQ
54	010003DC	E28D0C00	ADD RO,SP,#0xD000	FETCH_S_W	SEQ
55	010003E0	E95D0380	LDMEA SP,[R7-R9]A	FETCH_S_W	SEQ
56	010003E4	E12900F0	STRSH RO,[R9,-RO]!	FETCH_S_W	SEQ
57	010003E8	E1A00000	MOV RO,RO	FETCH_S_W	NONSEQ
58	0007EDF4	00000000	(32bit DATA READ)	READ_S_W	SEQ
59	0007EDF8	00000000	(32bit DATA READ)	READ_S_W	SEQ
60	0007EDFC	0100E464	(32bit DATA READ)	READ_S_W	ADDRESS
61	010003EC	0100E464	(32bit DATA READ)	READ_S_W	NONSEQ
62	010064E4	E4004600	B 01017CEC	FETCH_S_W	SEQ
63	010064E8	E1A00DC0	(FLUSH)	FETCH_S_W	SEQ
64	010064EC	E92D3008	(FLUSH)	FETCH_S_W	NONSEQ
65	01006604	E1A00DC0	MOV RO,RO,ASR #27	FETCH_S_W	SEQ
66	01006608	E92D7008	STMFD SP!,[R3-R4,R6-R7,R12-R15]	FETCH_S_W	SEQ
67	0100660C	E24C0480	SUB RO,IP,#0xB0000000	FETCH_S_W	SEQ
68	01006610	E15D0A00	CMP SP,RO,LSL #20	FETCH_S_W	NONSEQ
69	0007EDE4	00000000	(32bit DATA WRITE)	WRITE_U_W	SEQ
70	0007EDF0	00000000	(32bit DATA WRITE)	WRITE_U_W	SEQ

Depending on the complexity of the microprocessor or bus supported, there can be several display options that allow customization of the data display. These option selections can be found under the Disassembly tab of the Listing display properties menu. To go to this menu place the mouse pointer anywhere in the Listing data and click the right mouse button. Select the Properties choice from the pop-up list.

FIGURE 7. Disassembly Table of Listing display property

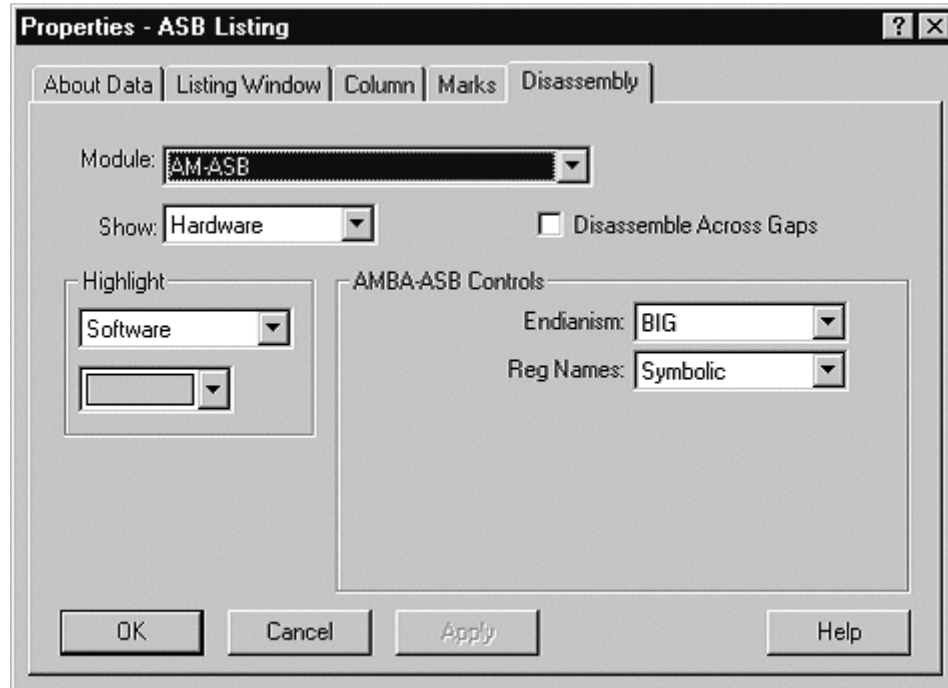


Figure 7 shows the Disassembly page (tab) of Listing display properties menu. In this example there are selectable fields for specific AM-ASB control:

- | | |
|-----------|--|
| Endianism | has two choices: BIG and little. This option is related to the Thumb instruction set. Thumb instructions may appear on most significant half word first (BIG) or on least significant halfword (little). |
| Reg Names | has two choices: Symbolic, or Rnumber. ARM registers are either represented in a range from R0 to R15 or as symbolic names (PC, SP, IP etc.). |

The **Show** field has four choices: Hardware, Software, Control Flow, and Subroutine. The selection in this field will alter the manner in which the Listing display shows data. Briefly, the four selections filter data as follows:

- | | |
|--------------|--|
| Hardware | This format selection shows all acquired processor or bus cycle types and instruction mnemonics in the order they occurred. |
| Software | This format selection suppresses all opcode extensions and flushed cycles and displays a menu that looks similar to an assembly language program listing. On version 2.0 TLA's and above, this format is to be used whenever a correlation with a Source window is wanted. |
| Control Flow | Only instructions that change the control flow of the microprocessor will be displayed. Instructions such as branches, calls, returns, etc. |
| Subroutine | Displays only subroutine calls, exceptions, and returns. |

Displaying Timing Data

A timing or waveform view of the data can be seen in the Waveform display. In addition to displaying the data collected in the main logic analyzer memory, the Waveform display allows you to add the high resolution 2GHz data collected by the MagniVu memory to the timing diagram display.

FIGURE 8. Typical Waveform display



If You Need Assistance

Support is available through Dragonfly Software Development. For package information and frequently asked questions, visit our Web site at www.dfsw.com. For technical assistance, contact us via e-mail at support@dfsw.com, or by phone during normal business hours at (877) 641-3440 (Pacific Time).

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