



TLA700 Series ARM7T

Microprocessor Support Instructions

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1. Overview

The TLA700 ARM7T Microprocessor Support Package adds support for ARM7T-based microprocessors to the TLA700. This manual describes the features of the ARM7T support package, package installation and configuration information, and guidelines for connecting the TLA700 to the system under test.

1.1. Support Description

The TLA700 ARM7T Microprocessor Support Package provides timing analysis, state analysis and both ARM and Thumb disassembly support for ARM7T microprocessor cores. This package is designed to capture and analyze the bus activity of an ARM7T processor.

Since the ARM7T is a microprocessor core, it is not possible to provide a support package that will work correctly with all possible ARM7T configurations, due to specific ASIC implementation differences which might arise. However, this support is compatible with the ARM7T specification, and is designed to operate directly on the ARM PID7T development board, as well as other boards that provide access to the required address, data and bus control signals.

The ARM7T package runs on TLA700 mainframes equipped with logic analyzer modules that are 102 channels or wider. At the time this manual was printed, the supported TLA700 logic analysis modules include the TLA7L3, TLA7M3, and TLA7N3 102 channel modules, and the TLA7L4, TLA7M4, TLA7N4 and TLA7P4 136 channel modules.

1.2. Support Features

This support package is designed to operate on the ARM7T bus. In addition to the timing and state analysis capabilities which are available with the TLA700, this package provides disassembly support for both ARM and Thumb instructions, in both little and big endian modes. ARM/Thumb detection is automatic.

1.3. Support Required Signals

The following signals should be provided to the logic analyzer module in order to support the ARM7T:

SIGNAL	REQUIRED?	EFFECT IF SIGNAL(S) NOT AVAILABLE
MCLK	Strongly Recommended	Internal or External clocking must be used to acquire bus cycles.
nWAIT	Strongly Recommended	Bus wait states will be acquired and disassembled, even though the bus cycle is not appropriate for disassembly.
nMREQ	Recommended	Internal and coprocessor cycles will be acquired and disassembled, even though the bus cycle is not appropriate for disassembly.
D[31-0]	Yes	No disassembly.
A[31-2]	Optional	Disassembled address values will be incorrect.
A[1]	Strongly Recommended	Disassembly of Thumb instructions and display of 16-bit data transfers will be inaccurate.
A[0]	Recommended	Display of 8-bit data transfers will be inaccurate.
MAS[1:0]	Strongly Recommended	ARM/Thumb disassembly support is degraded, as is identification of data transfer sizes.
nRW	Recommended	Data transfer direction misidentified.
nOPC	Strongly Recommended	No automatic detection of instruction fetch bus cycles.

2. Configuring the TLA700

2.1. Installing the ARM7T Support

Place the ARM7T installation disk in the TLA700 mainframe floppy disk drive. Click on the Windows 95 Start icon and select the Windows Explorer program. Click on the 3 1/2" Floppy icon to see the contents of the application software installation disk, and then double-click on the Setup.exe file to start the installation process.

The installation program will automatically install the package software into the appropriate folders in the TLA700 file system. For the ARM7T package, the support files will be installed into the "C:/Program Files/TLA700/Supports/Arm7t" folder.

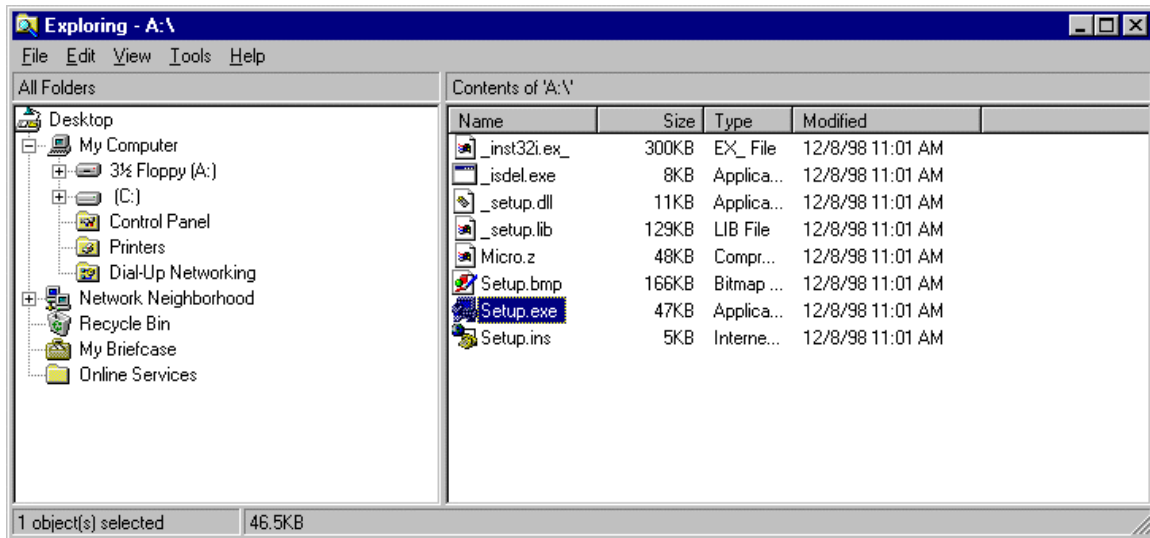


Figure 1: Double-click on the Setup.exe icon to install the software

2.2. Loading the ARM7T Support

To Load the ARM7T support package you must first select the logic analysis module that will be connected to the ARM7T bus under test. In the TLA700 System menu, select the logic analysis module you will be using by clicking on the title bar (labeled LA 1 below). This field will be renamed to the name of the supported microprocessor, in this case **ARM7T**, after successfully loading the support software.

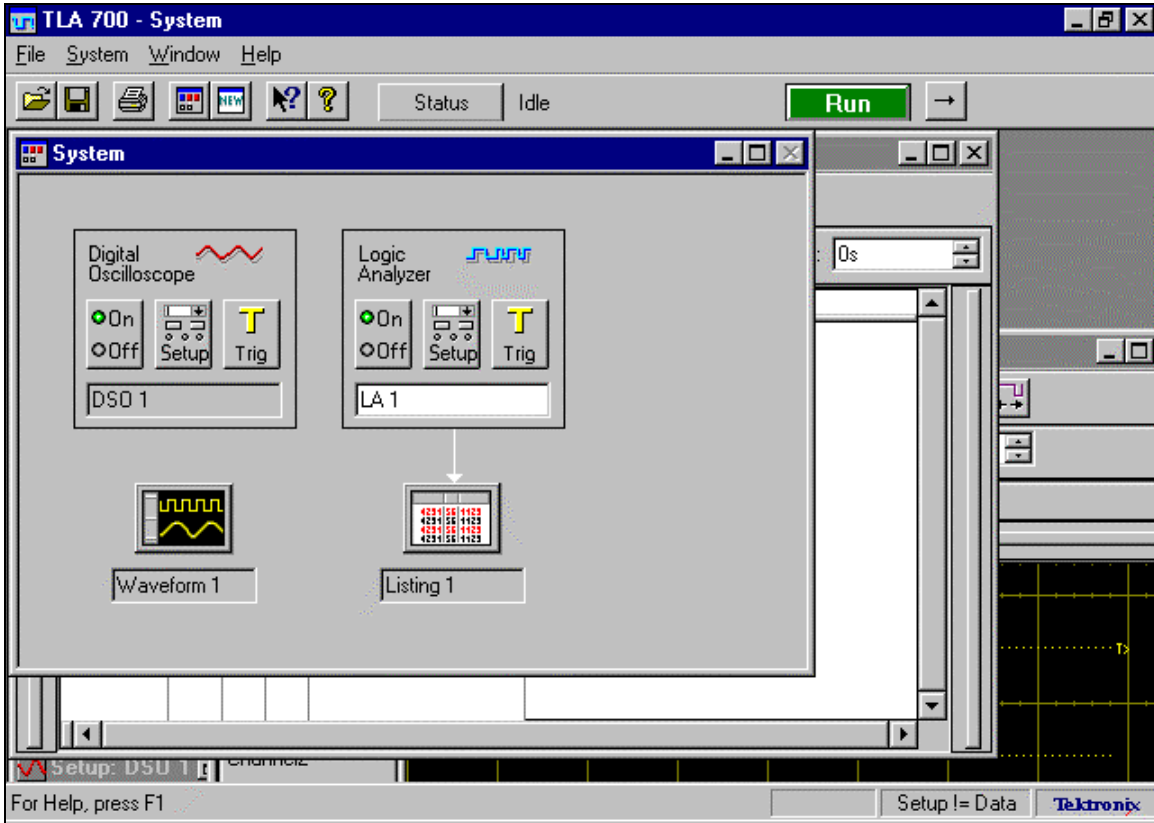


Figure 2: Selecting the logic analysis module for loading ARM7T support software.

Now click on **File** in the toolbar and select the **Load Support Package** option. The menu shown in Figure 3 will pop up on screen, allowing you to pick the support package you wish to load into the logic analysis module. Note that the list of support packages shown will depend on which microprocessor support applications you have previously loaded into the TLA700.

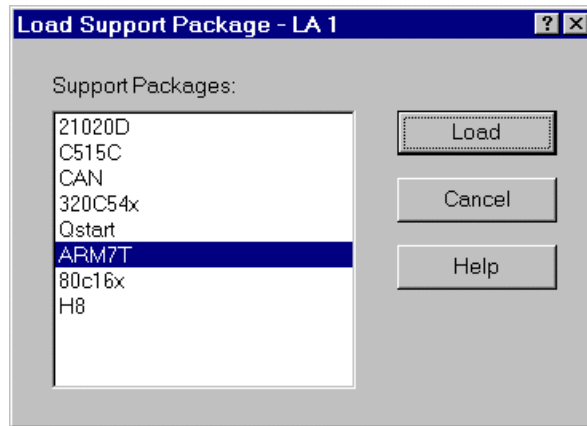


Figure 3: Load Support Package Dialog Box

Select **ARM7T** from the list of available support packages, and then click on the **Load** button. A dialog box with the following text will appear on screen:

“Loading a support package invalidates a module’s acquired data. Do you wish to save the current module’s settings and data before loading the support package?”

If you choose **Yes**, a “Save As...” file dialog box will appear, allowing you to save your current module setup or setup and data. Selecting **No** will cause the TLA700 to overwrite your current setup and data with the support package setup.

Clicking on the Setup button for the logic analysis module will take you to the Setup menu shown in Figure 4. Note that all of the input channels to be connected to the microprocessor bus have already been grouped and named.

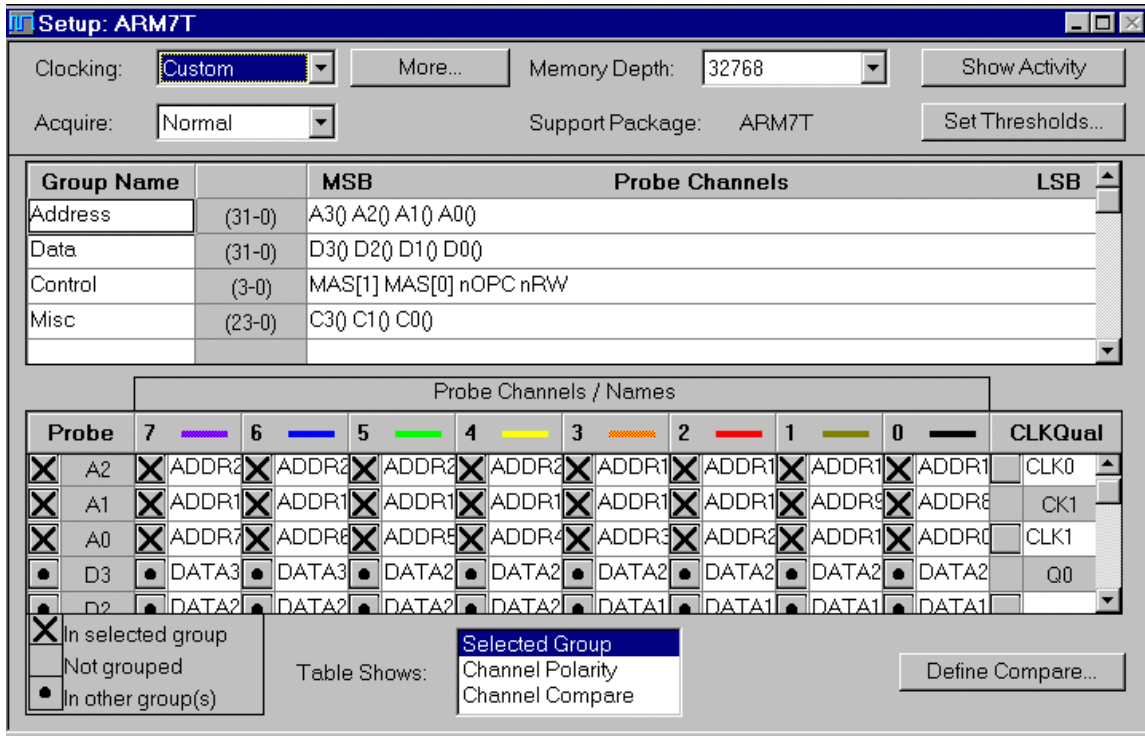


Figure 4: Logic analysis module setup after support has been loaded

2.3. Connecting to the ARM7T Bus

Due to different and specific physical packages of the integrated circuit embedding the ARM7T microprocessor core, it isn't possible to provide a general-purpose probe adapter that can connect to all possible systems.

When using the ARM PID7T board, connection is made to the ARM7T bus using the board POD connectors on the microprocessor daughtercard, using standard P6417 flying leadsets accessories for the POD1 through POD5 connectors. If Tektronix UPIK3M adapters are available, these can be used to simplify the connection to the ARM7T address bus and data bus (POD1 through POD4). The pinouts for the POD connectors, and their connections to the P6417 flying leadsets are described in Appendix A.

If P6434 Mictor probes are available, connection to the POD1 through POD4 connectors can be simplified using NEX-HD20 adapters from New Wave PDG. Contact New Wave PDG, at <http://www.busboards.com> for adapter specifications and ordering information.

Whenever possible, it is strongly suggested that either Mictor connectors (for P6434 probes) or square pins (for P6417 probes) be provided directly on the target board. The Mictor connector is described in Tektronix document 070-9793-02, available from Tektronix, at <http://www.tek.com>.

2.4. Clocking Options for ARM7T Support

The ARM7T Microprocessor Support Package provides several customized clocking options that are tailored to the characteristics of the ARM7T bus. Clicking on the **More...** button shown in the Setup menu in Figure 4 will take you to the Custom Clocking Options dialog box, shown below in Figure 5.

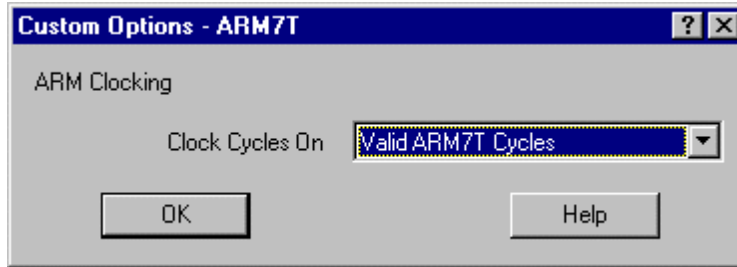


Figure 5: Custom Clock Options dialog box.

The following clocking options are available:

- **Valid ARM7T Cycles** This is the most commonly used of the clocking options, and is recommended for most ARM7T implementations. With this clocking option, nWAIT is utilized to suppress bus wait state cycles, and nMREQ is utilized to suppress internal and coprocessor bus cycles.
- **Valid PID7T Cycles** This clocking option is identical to “Valid ARM7T Cycles”, except that ‘nWAIT’ is treated as an active-high signal.
- **Simplified ARM7T Cycles** This clocking option is identical to “Valid ARM7T Cycles”, except that nMREQ is not utilized to suppress internal and coprocessor bus cycles.
- **Simplified PID7T Cycles** This clocking option is identical to “Simplified ARM7T Cycles”, except that ‘nWAIT’ is treated as an active-high signal.
- **Both Edges of MCLK** This clocking option samples the address, control, and data groups on both the rising and falling edges of MCLK. This clocking option is useful for debugging purposes, and can be used along with the Waveform displays of the TLA to study low-level ARM7T bus activity.

The following signals are required for each clocking option:

Custom Clocking Option	MCLK	nWAIT	nMREQ
Both Edges of MCLK	✓		
Simplified ARM7T Cycles	✓	✓	
Simplified PID7T Cycles	✓	✓	
Valid ARM7T Cycles	✓	✓	✓
Valid PID7T Cycles	✓	✓	✓

These clocking options should allow the support package to acquire relevant ARM7T bus activity in the majority of cases, but will not necessarily be appropriate for all implementations, due to implementation-specific differences in bus architecture, timing, etc. If a customized clocking method is required for a specific implementation, contract Dragonfly Software Development LLC for information about adding additional support to the package. See “If You Need Assistance” in section 6 for more information.

3. Channel Groups and Assignments

3.1. Address Group

ARM7T Group (Radix)	Group Bit Position, Section: Channel, & Channel Name			Voltage & Polarity	ARM7T Signal Name	PID7T POD/PIN	Mictor Conn./Pin
Address (Hex)	31	A3:7	ADDR 31	TTL,+	A(31)	POD4/4	A4
	30	A3:6	ADDR 30	TTL,+	A(30)	POD4/5	A5
	29	A3:5	ADDR 29	TTL,+	A(29)	POD4/6	A6
	28	A3:4	ADDR 28	TTL,+	A(28)	POD4/7	A7
	27	A3:3	ADDR 27	TTL,+	A(27)	POD4/8	A8
	26	A3:2	ADDR 26	TTL,+	A(26)	POD4/9	A9
	25	A3:1	ADDR 25	TTL,+	A(25)	POD4/10	A10
	24	A3:0	ADDR 24	TTL,+	A(24)	POD4/11	A11
	23	A2:7	ADDR 23	TTL,+	A(23)	POD4/12	A12
	22	A2:6	ADDR 22	TTL,+	A(22)	POD4/13	A13
	21	A2:5	ADDR 21	TTL,+	A(21)	POD4/14	A14
	20	A2:4	ADDR 20	TTL,+	A(20)	POD4/15	A15
	19	A2:3	ADDR 19	TTL,+	A(19)	POD4/16	A16
	18	A2:2	ADDR 18	TTL,+	A(18)	POD4/17	A17
	17	A2:1	ADDR 17	TTL,+	A(17)	POD4/18	A18
	16	A2:0	ADDR 16	TTL,+	A(16)	POD4/19	A19
	15	A1:7	ADDR 15	TTL,+	A(15)	POD3/4	A35
	14	A1:6	ADDR 14	TTL,+	A(14)	POD3/5	A34
	13	A1:5	ADDR 13	TTL,+	A(13)	POD3/6	A33
	12	A1:4	ADDR 12	TTL,+	A(12)	POD3/7	A32
	11	A1:3	ADDR 11	TTL,+	A(11)	POD3/8	A31
	10	A1:2	ADDR 10	TTL,+	A(10)	POD3/9	A30
	9	A1:1	ADDR 9	TTL,+	A(9)	POD3/10	A29
	8	A1:0	ADDR 8	TTL,+	A(8)	POD3/11	A28
	7	A0:7	ADDR 7	TTL,+	A(7)	POD3/12	A27
	6	A0:6	ADDR 6	TTL,+	A(6)	POD3/13	A26
	5	A0:5	ADDR 5	TTL,+	A(5)	POD3/14	A25
	4	A0:4	ADDR 4	TTL,+	A(4)	POD3/15	A24
	3	A0:3	ADDR 3	TTL,+	A(3)	POD3/16	A23
	2	A0:2	ADDR 2	TTL,+	A(2)	POD3/17	A22
	1	A0:1	ADDR 1	TTL,+	A(1)	POD3/18	A21
	0	A0:0	ADDR 0	TTL,+	A(0)	POD3/19	A20

3.2. Data Group

ARM7T Group (Radix)	Group Bit Position, Section: Channel, & Channel Name			Voltage, Polarity	ARM7T Signal Name	PID7T POD/PIN	Mictor Conn./Pin
Data (HEX)	31	D3:7	BD31	TTL,+	D(31)	POD2/4	D4
	30	D3:6	BD30	TTL,+	D(30)	POD2/5	D5
	29	D3:5	BD29	TTL,+	D(29)	POD2/6	D6
	28	D3:4	BD28	TTL,+	D(28)	POD2/7	D7
	27	D3:3	BD27	TTL,+	D(27)	POD2/8	D8
	26	D3:2	BD26	TTL,+	D(26)	POD2/9	D9
	25	D3:1	BD25	TTL,+	D(25)	POD2/10	D10
	24	D3:0	BD24	TTL,+	D(24)	POD2/11	D11
	23	D2:7	BD23	TTL,+	D(23)	POD2/12	D12
	22	D2:6	BD22	TTL,+	D(22)	POD2/13	D13
	21	D2:5	BD21	TTL,+	D(21)	POD2/14	D14
	20	D2:4	BD20	TTL,+	D(20)	POD2/15	D15
	19	D2:3	BD19	TTL,+	D(19)	POD2/16	D16
	18	D2:2	BD18	TTL,+	D(18)	POD2/17	D17
	17	D2:1	BD17	TTL,+	D(17)	POD2/18	D18
	16	D2:0	BD16	TTL,+	D(16)	POD2/19	D19
	15	D1:7	BD15	TTL,+	D(15)	POD1/4	D35
	14	D1:6	BD14	TTL,+	D(14)	POD1/5	D34
	13	D1:5	BD13	TTL,+	D(13)	POD1/6	D33
	12	D1:4	BD12	TTL,+	D(12)	POD1/7	D32
	11	D1:3	BD11	TTL,+	D(11)	POD1/8	D31
	10	D1:2	BD10	TTL,+	D(10)	POD1/9	D30
	9	D1:1	BD9	TTL,+	D(9)	POD1/10	D29
	8	D1:0	BD8	TTL,+	D(8)	POD1/11	D28
	7	D0:7	BD7	TTL,+	D(7)	POD1/12	D27
	6	D0:6	BD6	TTL,+	D(6)	POD1/13	D26
	5	D0:5	BD5	TTL,+	D(5)	POD1/14	D25
	4	D0:4	BD4	TTL,+	D(4)	POD1/15	D24
	3	D0:3	BD3	TTL,+	D(3)	POD1/16	D23
	2	D0:2	BD2	TTL,+	D(2)	POD1/17	D22
	1	D0:1	BD1	TTL,+	D(1)	POD1/18	D21
	0	D0:0	BD0	TTL,+	D(0)	POD1/19	D20

3.3. Control Group

ARM7T Group (Radix)	Group Bit Position, Section:Channel, Channel Name			Voltage, Polarity	ARM7T Signal Name	PID7T POD/PIN	Mictor Conn./Pin
Control (SYM)	3	C2:7	MAS[1]	TTL,+	MAS[1]	POD5/9	C12
	2	C2:6	MAS[0]	TTL,+	MAS[0]	POD5/10	C13
	1	C2:5	nOPC	TTL,+	nOPC	POD5/8	C14
	0	C2:4	nRW	TTL,+	nRW	POD5/11	C15
(not in group)		CK3	MCLK	TTL,+	MCLK	POD5/3	C3
		C2:1	nWAIT	TTL,+	nWAIT	POD5/18	C18
		C2:0	nMREQ	TTL,+	nMREQ	POD5/13	C19

3.4. Notes about Grounding

The ground connections for the Address, Data, and Control sections can be made on VSS. For the PID7T board, PIN 20 of each POD can be used for VSS.

4. Symbol Tables

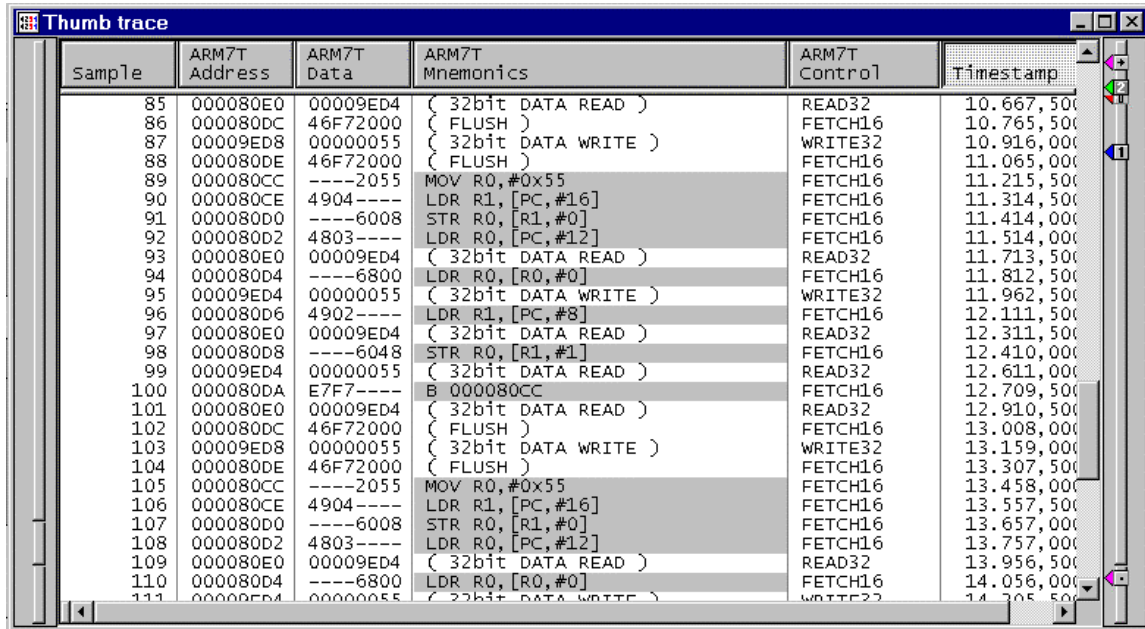
A symbol table for the Control group is included with this support package. The Control symbol table contains patterns that identify the type of valid bus transaction cycles for the symbolic disassembly. This symbol table is automatically selected for use in defining Control group patterns in the logic analyzer module's trigger menu.

Symbol Name	Signals	Description
	MAS[1] MAS[0] nOPC nRW	
FETCH32	1 0 0 0	32 bit Instruction fetch (ARM mode)
READ32	1 0 1 0	32 bit data read
WRITE32	1 0 1 1	32 bit data write
FETCH16	0 1 0 0	16 bit instruction fetch (THUMB mode)
READ16	0 1 1 0	16 bit data read
WRITE16	0 1 1 1	16 bit data write
FETCH8	0 0 0 0	8 bit instruction fetch
READ8	0 0 1 0	8 bit data read
WRITE8	0 0 1 1	8 bit data write
ARMSYMBOL	X X X X	Undefined

5. Disassembly & Timing Analysis

5.1. Displaying Disassembled Data

Once the ARM7T support package has been loaded into the TLA700, the Listing display for the logic analysis module will automatically display disassembled data. Figure 6 shows an example of disassembled data for an ARM7T microprocessor on ARM7T:



Sample	ARM7T Address	ARM7T Data	ARM7T Mnemonics	ARM7T Control	Timestamp
85	000080E0	00009ED4	(32bit DATA READ)	READ32	10.667,500
86	000080DC	46F72000	(FLUSH)	FETCH16	10.765,500
87	00009ED8	00000055	(32bit DATA WRITE)	WRITE32	10.916,000
88	000080DE	46F72000	(FLUSH)	FETCH16	11.065,000
89	000080CC	----2055	MOV R0,#0x55	FETCH16	11.215,500
90	000080CE	4904----	LDR R1,[PC,#16]	FETCH16	11.314,500
91	000080D0	----6008	STR R0,[R1,#0]	FETCH16	11.414,000
92	000080D2	4803----	LDR R0,[PC,#12]	FETCH16	11.514,000
93	000080E0	00009ED4	(32bit DATA READ)	READ32	11.713,500
94	000080D4	----6800	LDR R0,[R0,#0]	FETCH16	11.812,500
95	00009ED4	00000055	(32bit DATA WRITE)	WRITE32	11.962,500
96	000080D6	4902----	LDR R1,[PC,#8]	FETCH16	12.111,500
97	000080E0	00009ED4	(32bit DATA READ)	READ32	12.311,500
98	000080D8	----6048	STR R0,[R1,#1]	FETCH16	12.410,000
99	00009ED4	00000055	(32bit DATA READ)	READ32	12.611,000
100	000080DA	E7F7----	B 000080CC	FETCH16	12.709,500
101	000080E0	00009ED4	(32bit DATA READ)	READ32	12.910,500
102	000080DC	46F72000	(FLUSH)	FETCH16	13.008,000
103	00009ED8	00000055	(32bit DATA WRITE)	WRITE32	13.159,000
104	000080DE	46F72000	(FLUSH)	FETCH16	13.307,500
105	000080CC	----2055	MOV R0,#0x55	FETCH16	13.458,000
106	000080CE	4904----	LDR R1,[PC,#16]	FETCH16	13.557,500
107	000080D0	----6008	STR R0,[R1,#0]	FETCH16	13.657,000
108	000080D2	4803----	LDR R0,[PC,#12]	FETCH16	13.757,000
109	000080E0	00009ED4	(32bit DATA READ)	READ32	13.956,500
110	000080D4	----6800	LDR R0,[R0,#0]	FETCH16	14.056,000
111	00009ED4	00000055	(32bit DATA WRITE)	WRITE32	14.205,500

Figure 6: ARM7T Disassembled data display on the ARM7T bus

Depending on the complexity of the microprocessor or bus supported, there can be several display options that allow customization of the data display. These option selections can be found under the Disassembly tab of the Listing display properties menu. To go to this menu place the mouse pointer anywhere in the Listing data and click the right mouse button. Select the **Properties** choice from the pop-up list.

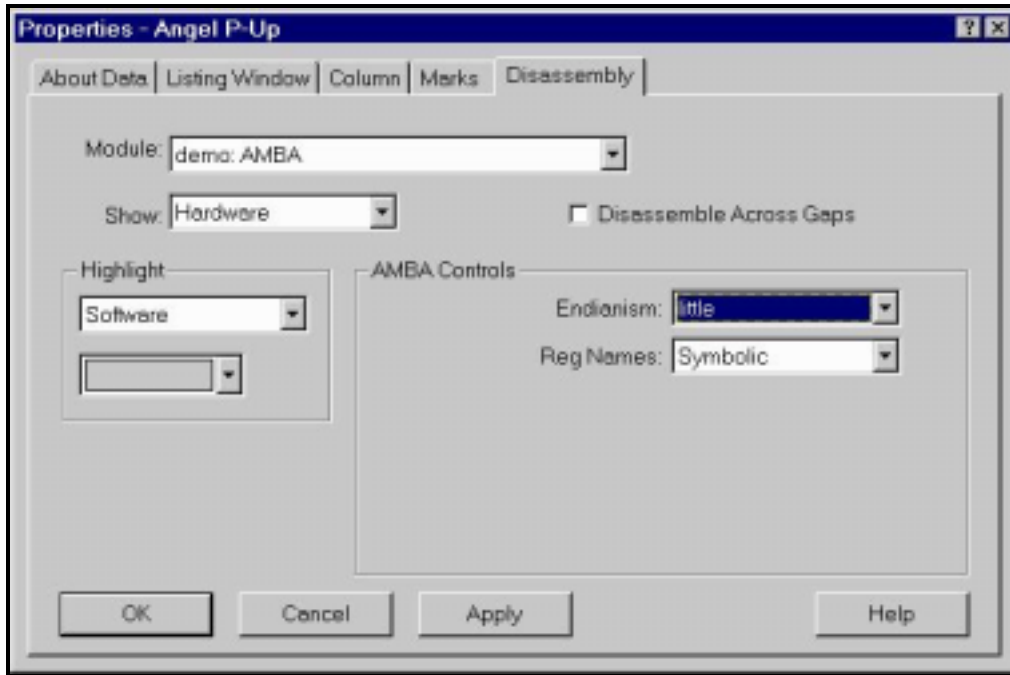


Figure 7: Disassembly Table of Listing display property

Figure 7 shows the Disassembly page (tab) of Listing display properties menu. In this example there are selectable fields for specific ARM7T control:

- **Endianism** has two choices: BIG and little. This option is related to the Thumb instruction set. Thumb instructions may appear on most significant half word first (BIG) or on least significant halfword (little).
- **Reg Names** has two choices: Symbolic, or Rnumber. ARM registers are either represented in a range from R0 to R15 or as symbolic names (PC, SP, IP etc.).

The **Show** field has four choices: Hardware, Software, Control Flow, and Subroutine. The selection in this field will alter the manner in which the Listing display shows data. Briefly, the four selections filter data as follows:

- **Hardware:** This format selection shows all acquired processor or bus cycle types and instruction mnemonics in the order they occurred.
- **Software:** This format selection suppresses all opcode extensions and flushed cycles and displays a menu that looks similar to an assembly language program listing. On version 2.0 TLA's and above, this format is to be used whenever a correlation with a Source window is wanted.
- **Control Flow:** Only instructions that change the control flow of the microprocessor will be displayed. Instructions such as branches, calls, returns, etc.
- **Subroutine:** Displays only subroutine calls, exceptions, and returns.

5.2. Displaying Timing Data

A timing or waveform view of the data can be seen in the Waveform display. In addition to displaying the data collected in the main logic analyzer memory, the Waveform display allows you to add the high resolution 2GHz data collected by the MagniVu memory to the timing diagram display.

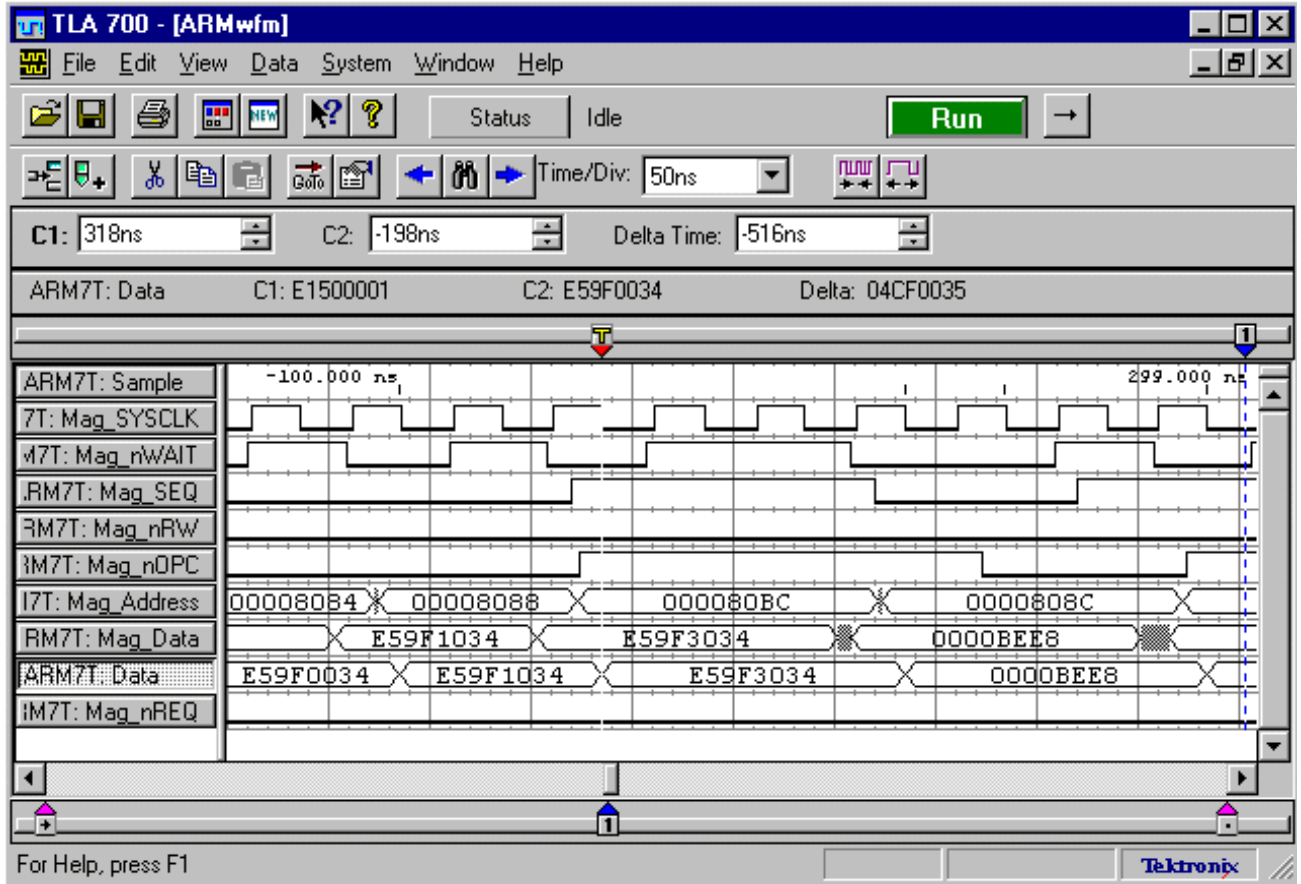


Figure 8: Typical Waveform display

6. If You Need Assistance

Support for the ARM7T Microprocessor Support Package is available through Dragonfly Software Development LLC. For package information and frequently asked questions, visit our Web site at www.dfsw.com. For technical assistance, you can contact us via e-mail at support@dfs.com, or by phone during normal business hours at (503) 641-3440 (Pacific Time).

Appendix A: PID7T Daughtercard Connections

POD1

NC	NC	1	2	VDD	NC
NC	NC	3	4	D[15]	D1:7
D1:6	D[14]	5	6	D[13]	D1:5
D1:4	D[12]	7	8	D[11]	D1:3
D1:2	D[10]	9	10	D[9]	D1:1
D1:0	D[8]	11	12	D[7]	D0:7
D0:6	D[6]	13	14	D[5]	D0:5
D0:4	D[4]	15	16	D[3]	D0:3
D0:2	D[2]	17	18	D[1]	D0:1
D0:0	D[0]	19	20	VSS	D0 gnd

POD2

NC	NC	1	2	VDD	NC
NC	NC	3	4	D[31]	D3:7
D3:6	D[30]	5	6	D[29]	D3:5
D3:4	D[28]	7	8	D[27]	D3:3
D3:2	D[26]	9	10	D[25]	D3:1
D3:0	D[24]	11	12	D[23]	D2:7
D2:6	D[22]	13	14	D[21]	D2:5
D2:4	D[20]	15	16	D[19]	D2:3
D2:2	D[18]	17	18	D[17]	D2:1
D2:0	D[16]	19	20	VSS	D2 gnd

POD3

NC	NC	1	2	VDD	NC
NC	NC	3	4	A[15]	A1:7
A1:6	A[14]	5	6	A[13]	A1:5
A1:4	A[12]	7	8	A[11]	A1:3
A1:2	A[10]	9	10	A[9]	A1:1
A1:0	A[8]	11	12	A[7]	A0:7
A0:6	A[6]	13	14	A[5]	A0:5
A0:4	A[4]	15	16	A[3]	A0:3
A0:2	A[2]	17	18	A[1]	A0:1
A0:0	A[0]	19	20	VSS	A0 gnd

POD4

NC	NC	1	2	VDD	NC
NC	NC	3	4	A[31]	A3:7
A3:6	A[30]	5	6	A[29]	A3:5
A3:4	A[28]	7	8	A[27]	A3:3
A3:2	A[26]	9	10	A[25]	A3:1
A3:0	A[24]	11	12	A[23]	A2:7
A2:6	A[22]	13	14	A[21]	A2:5
A2:4	A[20]	15	16	A[19]	A2:3
A2:2	A[18]	17	18	A[17]	A2:1
A2:0	A[16]	19	20	VSS	A2 gnd

POD5

	NC	1	2	VDD	
CLK3	MCLK	3	4	nEXEC	
	PIPEF	5	6	nM[1]	
	nM[0]	7	8	nOPC	C2:5
C2:7	MAS[1]	9	10	MAS[0]	C2:6
C2:4	nRW	11	12	SEQ	
C2:0	nMREQ	13	14	ABORT	
	nIRQ	15	16	nFIQ	
	nRESET	17	18	PWAIT	C2:1
	TBIT	19	20	VSS	C2 gnd

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